Abstract

An integrated circuit or other type of digital system including multiple processors is tested using a control mechanism which dynamically defines a group of processors subject to common control. The control mechanism receives one or more commands for each of the processors in the group, and delays issuance of one or more of the commands for the group until a designated group scan command is received for each of the processors in the group. The control mechanism may be in the form of a software-implemented chain manager which provides the above-noted group definition, command receipt and issuance delay operations, and subsequently delivers one or more of the test commands as a single serial bit stream to an IEEE 1149.1 hardware scan chain associated with the processors. The control mechanism can provide synchronous control for a group of homogeneous processors of the digital system, or pseudo-synchronous control for a group of heterogeneous processors of the digital system.